REMARKS

Claims 1-20 are pending in this application, of which claims 1-18 and 20 have been amended. No new claims have been added.

(1) Claims 1, 3, 5, 7, 9, 11, 13, 15 and 19 were rejected under 35 U.S.C. 102(e) as being anticipated by Kumar et al. (U.S. Patent No. 6,696,365).

(i) Kumar et al. teach a method for fabricating a semiconductor device comprising the steps of: forming a silicon oxide layer 12 on a silicon substrate 10; forming a silicon nitride layer 14 on the silicon oxide layer 12; forming a silicon oxide hardmask layer 16 on the silicon nitride layer 14; forming a polysilicon hardmask layer 18 on the silicon oxide hardmask layer 16; forming an antireflection layer 20 on the polysilicon hardmask layer 18; forming a photoresist film 22 on the antireflection layer 20; forming an opening in the photoresist film 22; etching the antireflection layer 20 and the polysilicon hardmask layer 18 with the photoresist film 22 as a mask; etching the silicon oxide hardmask layer 16, the silicon nitride layer 14 and the silicon oxide layer 12 with the polysilicon hardmask layer 18 as a mask; and etching the silicon substrate 10 with the silicon oxide hardmask layer 16, the silicon nitride layer 14 and the silicon oxide layer 12 as a mask (see Figs. 1-6).

In the invention of Kumar et al., the silicon oxide film 16, the silicon nitride film 14 and the silicon oxide film 12 are etched with the semiconductor film 18 as the mask (see Fig 4), and the silicon substrate 10 is etched with the silicon oxide film 16, the silicon nitride film 14 and the silicon oxide film 12 as the mask (see Fig. 6).

(ii) On the other hand, the silicon nitride film 14 of the present invention is etched with the semiconductor film 16 as a mask (see Fig. 2B of the present application), and the semiconductor substrate 10 is etched with the silicon nitride film 14 as a mask.

Thus, since the silicon nitride film 14 of the present invention is etched with the semiconductor film 16 as the mask, the silicon nitride film 14 is etched with high selectivity to the semiconductor film 16. Since the silicon nitride film 14 is etched with high selectivity to the semiconductor film 16, it is possible to prevent shoulders of a pattern of the silicon nitride film 14 from being largely etched. The present invention can form the pattern of the silicon nitride film 14 in a required configuration, so that the trenches can be formed in a required configuration. Therefore, the present invention can provide micronized semiconductor devices with high fabrication yields. Kumar et al., do not disclose nor suggest the features of the present invention.

(iii) The method disclosed in Kumar et al. would have the same problems as the method disclosed in Fig. 7 of JP 2000-269192 (Patent Reference 1) which is discussed at page 18, line 9 to page 19, line 16 of the specification of the present application.

Since the silicon oxide film 16 of Kumar et al. is etched with the semiconductor film 18 as a mask, the silicon oxide film 16 is not etched with high selectivity to the semiconductor film 18. Since the silicon oxide film 16 is not etched with high selectivity to the semiconductor film 18, shoulders of a pattern of the silicon oxide film 16, the silicon nitride film 14 and the silicon oxide film 12 are etched largely. Therefore, the invention of Kumar et al. cannot form the trenches in a required configuration.

(2) Claims 2, 4, 6, 8, 10, 12, 14, 16 and 20 were rejected under 35 U.S.C.§103(a) as being unpatentable over Kumar et al. in view of Shin (U.S. Patent Publication No. 2002/0024111).

The Examiner admits that Kumar et al. do not teach burying a second insulation film in the trenches, but states that Shin teaches burying a second insulation film 17 in the trenches (see Fig. 1).

However, Shin merely discloses burying the insulation film 17 in the trenches. As discussed above, the silicon nitride film 14 of the present invention is etched with the semiconductor film 16 as a mask (see Fig. 2B of the present application), and the semiconductor substrate 10 is etched with the silicon nitride film 14 as a mask. Thus, neither of the references discloses nor suggests modifying the disclosure into the features of the present invention, and even the combination of the reference does not make the present invention.

(3) Claim 17 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. in view of Shin and further in view of Trivedi (U.S. Patent Publication No. 2002/0019114).

The Examiner states that Trivedi teaches forming an insulation film 48 in the trenches 31 and on the first insulation film 29 and chemical-mechanical-polishing the second insulation film 48 until the first insulation film 29 is exposed.

However, Trivedi merely discloses burying the element isolation regions 48 in the trenches 31. As discussed above, the silicon nitride film 14 of the present invention is etched with the semiconductor film 16 as a mask (see Fig. 2B of the present application), and the semiconductor substrate 10 is etched with the silicon nitride film 14 as a mask. None of the cited references discloses nor suggests the features of the present invention.

(4) Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. in view of Shin and further in view of Trivedi.

The Examiner states that Travedi teaches etching off the first insulation film 29 (Figs. 8 and 9); and forming a gate insulation film over the semiconductor substrate 27 (Fig. 10). However, Travedi merely discloses etching off the first insulation film 29 and forming the gate insulation film. As discussed above, the silicon nitride film 14 of the present invention is etched with the semiconductor film 16 as a mask (see Fig. 2B of the present application), and the semiconductor substrate 10 is etched with the silicon nitride film 14 as a mask. Thus, none of the cited references discloses nor suggests the features of the present invention.

(5) In view of the above, claims 1-20, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned representative at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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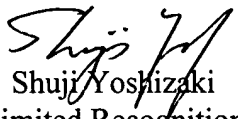

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